Remarks

Applicants thank the Examiner for the careful examination of this application and the clear explanation of the rejections.

The new claims obviate the rejections under 35 USC 103. The amended and new claims "particularly point out and distinctly claim the subject matter the applicant regards as his invention."

New claim 22 defines an RF receiver integrated circuit.

There is a substrate of semiconductor material

Mixer circuitry, formed on the substrate, has an input for receiving an analog RF signal with a bandwidth of f_o and an output for supplying an analog IF signal of frequency f_c in response to receiving the analog RF signal.

Analog to digital converter circuitry, formed on the substrate, has an input connected with the output of the mixer circuitry and has four parallel outputs carrying signals representing a digital IF signal. The converter circuitry has a sampling frequency f_s of four times f_c.

CORDIC circuitry, formed on the substrate, has four parallel inputs connected with the four parallel outputs of the converter circuitry, a first set of four outputs, and a second set of four outputs.

First decimator and quantizer circuitry, formed on the substrate, has inputs connected with the first set of four outputs and an output of two bits supplying signals at a sampling frequency of $2xf_o$.

Second decimator and quantizer circuitry, formed on the substrate, has inputs connected with the second set of four outputs and an output of two bits supplying signals at a sampling frequency of $2xf_o$.

Multiplex and serial to parallel circuitry, formed on the substrate, has inputs connected with the outputs of the first and second decimator and quantizer circuitry and having a serial output.

First differential transmitter circuitry, formed on the substrate, has an input connected with the serial output and has first differential serial outputs for sending signals at a sampling rate of $8xf_o$ from the substrate.

In contrast, Applicants Admitted Prior Art (AAPA) discloses, in Figure 2, clock leads and signals and 2-bit A/D converter circuitry on one integrated circuit and on another integrated circuit Digital IF-to-BB Converter circuitry, Matched Filter Circuitry, and Digital Communication Processing circuitry. Complicated frequency divisions must occur to convey signals from the one integrated circuit to the other integrated circuit. A clock signal must also be conveyed from the one integrated circuit to the other integrated circuit.

This AAPA arrangement of circuitry on two different integrated circuits presents the frequency planning problems overcome by the claimed

RF receiver integrated circuit. The claimed RF receiver integrated circuit positively recites mixer circuitry, analog to digital converter circuitry, CORDIC circuitry, first decimator and quantizer circuitry, second decimator and quantizer circuitry, and multiplex and serial to parallel circuitry, all formed on the same substrate, for frequency planning to occur on only one integrated circuit and with first differential transmitter circuitry sending signals at a sampling rate of $8xf_o$ from the substrate.

The claimed RF receiver integrated circuit also positively recites an analog RF signal with a bandwidth of f_o, an analog IF signal of frequency f_c, a converter sampling frequency f_s of four times f_c, and decimator and quantizer circuitry output of two bits supplying signals at a sampling frequency of $2xf_o$.

The Troster paper discloses only an A-to-D converter and digital quadrature demodulator circuitry on one integrated circuit. Apparently there is no disclosure of any CORDIC circuitry connecting the A-to-D converter and demodulator circuitry and no mention of solving any problems in frequency planning between integrated circuits. Thus any suggestion of a single integrated circuit from the Troster paper leaves a person of ordinary skill with no direction on frequency planning. It also fails to suggest the separate first and second decimator and quantizer circuitries each connecting to the multiplex and parallel to serial converter circuitry.

The Williams patent, US 5,557,642 discloses adjusting the frequency of clock CLK1 at any desired frequency. No suggestion of frequency planning on one rather than between two integrated circuits occurs in the

Williams patent. It also fails to suggest the separate first and second decimator and quantizer circuitries each connecting to the multiplex and parallel to serial converter circuitry.

The Patel patent, US 6,480,528, discloses automatic gain control of multicarrier signals. No suggestion of frequency planning on one rather than between two integrated circuits occurs in the Patel patent. It also fails to suggest the separate first and second decimator and quantizer circuitries each connecting to the multiplex and parallel to serial converter circuitry.

The Fukuda patent, US 4,665,532, discloses an input signal divided into two sequences, which are then multiplied by cos ώt and sin ώt in the regenerative carrier waves in mixtures 202 and 203 for demodulation. The two sequences of baseband receiving signals obtained by this demodulation are supplied via low-pass filters 204 and 205 to a bit timing recovery (BTR) circuit 206 and analog to-digital (A/D) converters 207 and 208, respectively. In the BTR circuit 206, a clock frequency is regenerated. This regenerated clock is used for the A/D conversion in the A/D converters 207 and 208. The digital signals are frame-synchronized in a decoder 209, then the digital signals encoded in the transmitting system are obtained. The decoder signals are parallel/serial (P/S) converted in a P/S converter 210 for recovery of the transmitted data of the 45M bpsx2.

No suggestion of frequency planning on one rather than between two integrated circuits occurs in the Fukuda patent. It also fails to suggest the separate first and second decimator and quantizer circuitries each connecting

to the multiplex and parallel to serial converter circuitry. The Fukuda patent, Figure 2, depicts two outputs from the P/S 210.

The depending claims also stand allowable as depending from allowable independent claim and as including, in combination with the limitations of the independent claim, additional distinguishing limitations.

The depending claims add limitations of clock signal frequencies and details of serial transmitter circuitry and of serial receiver circuitry.

The disclosure of the Analog Devices AD9870 also fails to teach or suggest all of the limitations of the independent and depending claims.

The application is in allowable form and the claims distinguish over the cited references. Applicants respectfully request reconsideration or further examination of this application.

Respectfully Submitted,

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